Annealing temperature dependence of capacitance-voltage characteristics in Ge-nanocrystal-based nonvolatile memory structures


Citation: Journal of Applied Physics 99, 036101 (2006); doi: 10.1063/1.2168249
View online: http://dx.doi.org/10.1063/1.2168249
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/99/3?ver=pdfcov
Published by the AIP Publishing

Articles you may be interested in

Effect of annealing on charge transfer in Ge nanocrystal based nonvolatile memory structure

Large capacitance-voltage hysteresis loops in SiO2 films containing Ge nanocrystals produced by ion implantation and annealing

Structural and electrical properties of Ge nanocrystals embedded in SiO2 by ion implantation and annealing
J. Appl. Phys. 97, 104330 (2005); 10.1063/1.1909286

Introduction of Si/SiO2 interface states by annealing Ge-implanted films
J. Appl. Phys. 96, 4308 (2004); 10.1063/1.1790579

Electrical study of Ge-nanocrystal-based metal-oxide-semiconductor structures for p-type nonvolatile memory applications
Appl. Phys. Lett. 84, 5079 (2004); 10.1063/1.1751227

2014 Special Topics

PEROVSKITES   2D MATERIALS   MESOPOROUS MATERIALS   BIOMATERIALS/ BIOELECTRONICS   METAL-ORGANIC FRAMEWORK MATERIALS

Submit Today!
Annealing temperature dependence of capacitance-voltage characteristics in Ge-nanocrystal-based nonvolatile memory structures

C. J. Park\textsuperscript{a)\textsuperscript{a)} and H. Y. Cho
Department of Physics and Quantum-Functional Semiconductor Research Center, Dongguk University, Seoul 100-715, Korea
S. Kim and Suk-Ho Choi
Department of Physics and Applied Physics, College of Electronics and Information, Kyung Hee University, Yongin 449-701, Korea
R. G. Elliman
Electronic Materials Engineering Department, Research School of Physical Sciences and Engineering, Australian National University, Canberra ACT Australian Capital Territory 0200, Australia
J. H. Han and Chungwoo Kim
Devices Lab, Samsung Advanced Institute of Technology, Kiheung-eup, Yongin-city, Kyunggi-do 449-712, Korea
H. N. Hwang and C. C. Hwang
Beamline Research Division, Pohang Accelerator Laboratory, Pohang University of Science and Technology, Pohang, Kyungbuk 790-784, Korea

(Received 25 November 2005; accepted 16 December 2005; published online 7 February 2006)

The annealing temperature ($T_a$) dependence of capacitance-voltage ($C$-$V$) characteristics has been studied in metal-oxide-semiconductor structures containing Ge nanocrystals (NCs) produced by ion implantation and annealing. These structures are of interest for application as nonvolatile memory and $T_a$ is shown to have a strong influence on the $C$-$V$ hysteresis. This behavior is shown to be correlated with structural changes of the Ge NCs which have been characterized by synchrotron-radiation photoemission spectroscopy. Specifically, well-defined $C$-$V$ characteristics with large hysteresis were found only for annealing temperatures greater than 950 °C where Ge nanocrystals are known to form. In this temperature regime, transmission electron microscopy and energy dispersive x-ray spectroscopy demonstrate the existence of regularly arranged Ge NCs of approximately 3–5 nm diameter located around 6.7 nm from the interface. © 2006 American Institute of Physics. [DOI: 10.1063/1.2168249]

Over the past decade Si and Ge nanocrystals (NCs) embedded in insulating host materials have been the subject of intensive investigation as potential materials for electronic and optoelectronic device applications.\textsuperscript{1,2} One of the most exciting such applications is as nonvolatile memory (NVM) and the demonstration of nonvolatile NC memory operation at room temperature has further stimulated the interest in such materials.\textsuperscript{3,4} Indeed, several research groups have successfully fabricated high-quality NVM devices by employing Si or Ge NCs but each study shows different NVM characteristics without a detailed explanation for how the characteristics depend on the physical properties of the materials or the relative role of NCs and/or defects.

In principle, Ge NCs have greater potential than Si NCs to improve the NVM function because of their smaller energy band gap.\textsuperscript{5} Quantum confinement effects should also be greater in Ge than in Si because of its smaller electron and hole effective masses and larger dielectric constant.\textsuperscript{6} Charge storage in Ge–NC-based metal-oxide-semiconductor (MOS) structures is influenced by several mechanisms including quantum confinement/Coulomb blockade effects, and interface/defect states.\textsuperscript{5,7} A number of groups have published reports on the structural properties of Ge NCs,\textsuperscript{8,9} with the most detailed\textsuperscript{9} providing important insight into the effect of annealing on the evolution of Ge nanocrystals. However, it is very important to investigate such behavior in the context of the present study, especially in relation to the influence of the SiO$_2$/Si interface and the SiO$_2$/metal contact in MOS structures which may directly affect the NVM characteristics.

This letter reports on a detailed study of the effect of annealing on the formation of Ge nanocrystals and the development of well-defined capacitance-voltage ($C$-$V$) characteristics in MOS structures containing Ge NCs. This is undertaken by employing several experimental techniques, including $C$-$V$, transmission electron microscopy (TEM), synchrotron-radiation photoemission spectroscopy (SRPES), and energy dispersive x-ray spectroscopy (EDS).

SiO$_2$ layers with 30 nm thickness were grown on $n$-type (100) Si substrates in a conventional furnace. The SiO$_2$ layer was implanted with 30 keV Ge$^{+}$ to nominal fluences of $5.0 \times 10^{15}$ and $1.0 \times 10^{16}$ Ge cm$^{-2}$ at room temperature and subsequently annealed at temperatures in the range from 800 to 1050 °C for 10 min in an Ar atmosphere. The peak excess-Ge concentration for these implants was calculated,
FIG. 1. Annealing temperature dependence of C-V hysteresis loops for MOS structures with oxides implanted with Ge ions to fluences of (a) $1.0 \times 10^{16}$ and (b) $5.0 \times 10^{15}$ cm$^{-2}$. The C-V curve of an unimplanted sample is included for reference.

FIG. 2. (a) Cross-sectional TEM images and (b) EDS spectra for Ge implanted SiO$_2$ after annealing at 950 °C for 10 min. The implant fluence is $1.0 \times 10^{16}$ cm$^{-2}$ and Ge NCs are indicated by circles.

from TRIM simulation, to be around 6% and 11%, respectively. The density and size of Ge NCs were investigated by TEM and depth profile of Ge atoms was evaluated by EDS. To investigate the chemical structures of the surface region, SRPES measurements were carried out at the 7B1 beamline of Pohang Accelerator Laboratory. The SRPES data were taken at normal emission angle: $90^\circ$ with 170 eV photons. Al electrodes with a diameter of 300 μm were deposited on the samples in vacuum for C-V measurements, which were carried out at 300 K by using a Boonton 7200 capacitor meter to study the memory effects from Ge NCs in MOS capacitors.

Figure 1 compares the C-V hysteresis loops of MOS structures with oxides implanted with Ge ions to fluences of $1.0 \times 10^{16}$ and $5.0 \times 10^{15}$ cm$^{-2}$ and annealed at various temperatures. The hysteresis in the C-V curves can be attributed to the reversible storage of holes or electrons in the NCs based on quantum confinement and/or in the defect states at their interfaces with the SiO$_2$ matrix. If the stored charge is stable, the shift in the flatband voltage produces a corresponding shift in the threshold voltage, showing ideal hysteresis behavior, as shown for annealing temperatures ($T_A$) $\geq 950$ °C in Figs. 1(a) and 1(b). In some cases, oxides and SiO$_2$/Si or SiO$_2$/metal interfaces contain unstable charges that can be influenced by the applied voltage. In this case, the threshold voltage itself depends on the gate voltage. The C-V curve is then distorted, as shown at lower $T_A$'s in the insets in Figs. 1(a) and 1(b).

Figure 2 shows the cross-sectional TEM images and EDS signals of a 30 nm oxide implanted with Ge ions to a fluence of $1.0 \times 10^{16}$ cm$^{-2}$ and subsequently annealed at 950 °C. Figure 2(a) shows an array of dark spots indicating Ge NCs along Si/SiO$_2$ interface. The higher-resolution image confirms the presence of Ge NCs of approximately 3–4 nm in diameter, as indicated by circles in the inset. The average distance from the Si substrate to the Ge NC layer is estimated to be about 6.7 nm and the nanocrystal density is calculated as $2 \times 10^{12}$ cm$^{-2}$ from plane-view TEM images.

Figure 2(b) shows the EDS spectra from different depths in the direction from the SiO$_2$ surface to Si substrate. The analysis reveals only low Ge concentrations in the near-surface region of the sample and in the middle of SiO$_2$ layer [as indicated by 1 and 2 in Fig. 2(a)] but shows a high concentration of Ge at positions near the Ge NC layer and the SiO$_2$/Si interface [as indicated by 3 and 4 in Fig. 2(a)]. It is also evident that the peak ratio of Ge to O in the EDS spectra increases in the direction toward the Si/SiO$_2$ interface. These results are consistent with the fact that ion-implanted Ge has diffused during annealing and accumulated at the Si/SiO$_2$ interface.

Figure 3 shows the SRPES spectra of selected Si 2$p$ and Ge 3$d$ core levels for the samples implanted with a fluence of $1.0 \times 10^{16}$ cm$^{-2}$ as a function of $T_A$. Note that the analysis was performed on the sample surface and SRPES is only sensitive to a region of several-nanometer depth. The binding energy (103.3 eV) of the Si 2$p$ spectrum corresponds to Si in the SiO$_2$ phase as demonstrated in the previous reports. For the Ge 3$d$ level spectra have been previously been found to...
split into two components related to Ge–Ge and Ge–O bonds, respectively, but in this work only the signal from the Ge–O bond is observed, as shown in Fig. 3. The binding energy (30.8 eV) of the Ge 3d level is about 1.0 eV smaller than that of stoichiometric GeO$_2$. These considerations suggest the presence of an underoxidized GeO$_x$ structure without metallic Ge. Therefore, a mixture of SiO$_2$ and GeO$_x$ appears to exist in the near-surface region of the Ge-implanted oxide layer. The $T_A$ dependence of the two peaks is summarized in the inset of Fig. 3. With increasing $T_A$, the GeO$_x$ phase decreases and the SiO$_2$ phase increases. Similar behavior was observed for the samples implanted with a fluence of 5 $\times$ 10$^{15}$ cm$^{-2}$.

When Ge ions are implanted into SiO$_2$ films Si–O bonds are destroyed resulting in a mixture of Ge, Si, and O atoms. At low $T_A$'s, Ge–O (including GeO$_x$) bonds can be formed in addition to Si–O bonds. At high $T_A$'s, GeO$_x$ is reduced by Si to produce SiO$_2$ and Ge, consistent with the data in Fig. 3 and previous report. During this stage, Ge atoms diffuse throughout the layer and accumulate at the Si/SiO$_2$ interface, consistent with the EDS results in Fig. 2(b). The precipitation of Ge nanocrystals coincides with the onset of well-defined C–V curves, as shown in Figs. 1(a) and 3. The C–V curves of samples annealed at lower temperatures, inset in Fig. 1(a), are consistent with the fact that the mixed SiO$_2$/GeO$_x$ phase and/or defects in the oxide layer induce unstable charge at the SiO$_2$/metal interface.

The above analysis suggests that the presence of Ge NCs is important for establishing well-defined C–V characteristics and that the memory effect is therefore related to charges stored in Ge NCs. The existence of Ge NCs is confirmed by TEM, as shown in Fig. 2. Moreover, it is known that the formation temperature of Ge NCs is $\approx$850–900 °C, which is much lower than that of Si NCs. In Fig. 1, the samples annealed at $T_A$'s=900 °C show distorted C–V curves consistent with the lack of well defined nanocrystals. Therefore, it is necessary to anneal the Ge-implanted samples above 900 °C for well-defined C–V curves in Ge-NC-based NVM memories.

In conclusion, C–V, TEM, EDS, and SRPES were used to characterize MOS structures containing Ge NCs produced by ion-implantation and annealing. The C–V hysteresis curves were shown to depend strongly on $T_A$, with well-defined C–V curves being observed for $T_A \geqslant 950$ °C where Ge nanocrystals are known to form. In this regime TEM and EDS demonstrated the existence of regularly arranged Ge NCs of approximately 3–5 nm diameter located around 6.7 nm from the interface. This data provide strong support for the fact that the C–V hysteresis is dominated by charge trapping at Ge nanocrystals.

One of the authors (S.–H.C.) acknowledges the partial support from the National research program for the 0.1 Terabit Non-Volatile Memory Development sponsored by Korea Ministry of Science and Technology. Another author (H.Y.C.) also acknowledges partial supports from the Quantum-Functional Semiconductor Research Center in Dongguk University and the National Program for Tera level Nano Devices through MOST. Another author (R.G.E.) also acknowledges the Australian Research Council for their partial financial support of this research.